WIRELESS POWER CONSORTIUM

Qi Specification

Communications Physical Layer

Version 1.3

January 2021

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RELEASE HISTORY

Specification Version	Release Date	Description
1.3	January 2021	Initial release of this document.

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1 General

The Wireless Power Consortium (WPC) is a worldwide organization that aims to develop and promote global standards for wireless power transfer in various application areas. A first application area comprises flat-surface devices such as mobile phones and chargers in the Baseline Power Profile (up to 5 W) and Extended Power Profile (above 5 W).

1.1 Structure of the Qi Specification

General documents

- Introduction
- Glossary, Acronyms, and Symbols

System description documents

- Mechanical, Thermal, and User Interface
- Power Delivery
- Communications Physical Layer
- Communications Protocol
- Foreign Object Detection
- NFC/RFID Card Protection
- Authentication Protocol

Reference design documents

- Power Transmitter Reference Designs
- Power Receiver Design Examples

Compliance testing documents

- Power Transmitter Test Tools
- Power Receiver Test Tools
- Power Transmitter Compliance Tests
- Power Receiver Compliance Tests

NOTE: The compliance testing documents are restricted and require signing in to the WPC members' website. All other specification documents are available for download on both the WPC public website and the WPC website for members.

1.2 Scope

The *Communications Physical Layer* (this document) defines the low-level (physical layer and the data link layer) formats of data bits, data bytes, and data packets. In addition, it provides requirements and guidelines for load modulation and frequency-shift keying.

1.3 Compliance

All provisions in the *Qi Specification* are mandatory, unless specifically indicated as recommended, optional, note, example, or informative. Verbal expression of provisions in this Specification follow the rules provided in ISO/IEC Directives, Part 2.

Table 1: Verbal forms for expressions of provisions

Provision	Verbal form
requirement	"shall" or "shall not"
recommendation	"should" or "should not"
permission	"may" or "may not"
capability	"can" or "cannot"

1.4 References

For undated references, the most recently published document applies. The most recent WPC publications can be downloaded from http://www.wirelesspowerconsortium.com. In addition, the *Qi Specification* references documents listed below. Documents marked here with an asterisk (*) are restricted and require signing in to the WPC website for members.

- Product Registration Procedure Web page*
- Qi Product Registration Manual, Logo Licensee/Manufacturer*
- Qi Product Registration Manual, Authorized Test Lab*
- Power Receiver Manufacturer Codes,* Wireless Power Consortium
- The International System of Units (SI), Bureau International des Poids et Mesures
- Verbal forms for expressions of provisions, International Electotechnical Commission

For regulatory information about product safety, emissions, energy efficiency, and use of the frequency spectrum, visit the regulatory environment page of the WPC members' website.

1.5 Conventions

1.5.1 Notation of numbers

- Real numbers use the digits 0 to 9, a decimal point, and optionally an exponential part.
- Integer numbers in decimal notation use the digits 0 to 9.
- Integer numbers in hexadecimal notation use the hexadecimal digits 0 to 9 and A to F, and are prefixed by "0x" unless explicitly indicated otherwise.
- Single bit values use the words ZERO and ONE.

1.5.2 Tolerances

Unless indicated otherwise, all numeric values in the *Qi Specification* are exactly as specified and do not have any implied tolerance.

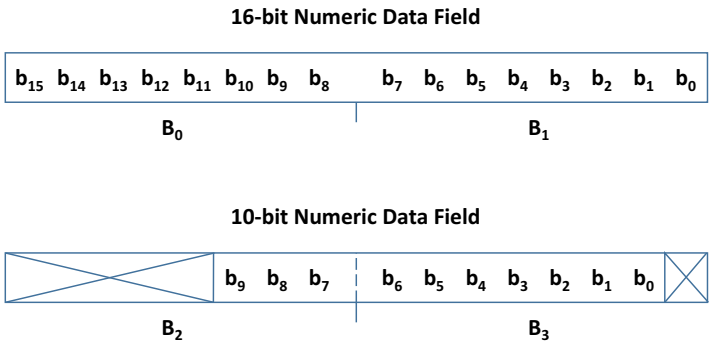
1.5.3 Fields in a data packet

A numeric value stored in a field of a data packet uses a big-endian format. Bits that are more significant are stored at a lower byte offset than bits that are less significant. Table 2 and Figure 1 provide examples of the interpretation of such fields.

Table 2: Example of fields in a data packet

	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
B_0	(msb) 16-bit Numeric Data Field							
B_1								(lsb)
B_2	Other Field					(msb)		
B_3	10-bit Numeric Data Field						(lsb)	Field

Figure 1. Examples of fields in a data packet



1.5.4 Notation of text strings

Text strings consist of a sequence of printable ASCII characters (i.e. in the range of 0x20 to 0x7E) enclosed in double quotes ("). Text strings are stored in fields of data structures with the first character of the string at the lowest byte offset, and are padded with ASCII NUL (0x00) characters to the end of the field where necessary.

EXAMPLE: The text string “WPC” is stored in a six-byte fields as the sequence of characters 'W', 'P', 'C', NUL, NUL, and NUL. The text string “M:4D3A” is stored in a six-byte field as the sequence 'M', ':', '4', 'D', '3', and 'A'.

1.5.5 Short-hand notation for data packets

In many instances, the *Qi Specification* refers to a data packet using the following shorthand notation:

<MNEMONIC>/<modifier>

In this notation, <MNEMONIC> refers to the data packet's mnemonic defined in the *Qi Specification, Communications Protocol*, and <modifier> refers to a particular value in a field of the data packet. The definitions of the data packets in the *Qi Specification, Communications Protocol*, list the meanings of the modifiers.

For example, EPT/cc refers to an End Power Transfer data packet having its End Power Transfer code field set to 0x01.

1.6 Power Profiles

A Power Profile determines the level of compatibility between a Power Transmitter and a Power Receiver. Table 3 defines the available Power Profiles.

- *BPP PTx*: A Baseline Power Profile Power Transmitter.
- *EPP5 PTx*: An Extended Power Profile Power Transmitter having a restricted power transfer capability, i.e. $P_L^{(pot)}$ = 5 W.
- *EPP PTx*: An Extended Power Profile Power Transmitter.
- *BPP PRx*: A Baseline Power Profile Power Receiver.
- *EPP PRx*: An Extended Power Profile Power Receiver.

Table 3: Capabilities included in a Power Profile

Feature	BPP PTx	EPP5 PTx	EPP PTx	BPP PRx	EPP PRx
A*x* or B*x* design	Yes	Yes	No	N/A	N/A
MP-A*x* or MP-B*x* design	No	No	Yes	N/A	N/A
Baseline Protocol	Yes	Yes	Yes	Yes	Yes
Extended Protocol	No	Yes	Yes	No	Yes
Authentication	N/A	Optional	Yes	N/A	Optional

2 Load Modulation

This section defines both the physical layer and the data link layer of the Power Receiver to Power Transmitter communications interface.

The Power Receiver communicates to the Power Transmitter using backscatter modulation. For this purpose, the Power Receiver modulates the amount of power that it draws from the Power Signal. The Power Transmitter detects this as a modulation of the current through and/or voltage across the Primary Cell. In other words, the Power Receiver and Power Transmitter use an amplitude modulated Power Signal to provide a Power Receiver to Power Transmitter communications channel.

2.1 Modulation scheme

The Power Receiver shall modulate the amount of power that it draws from the Power Signal, such that the Primary Cell current and/or Primary Cell voltage assume two states, namely a HI state and a LO state.[1] A state is characterized in that the amplitude is constant within a certain variation Δ for at least t_S ms. If the Power Receiver is properly aligned to the Primary Cell of a type A10 or MP-A1 Power Transmitter, and for all appropriate loads, at least one of the following three conditions shall apply:[2]

- The difference of the amplitude of the Primary Cell current in the HI and LO state is at least 15 mA.
- The difference of the Primary Cell current in the HI and LO state is at least 15 mA. The Primary Cell current is measured at instants in time that correspond to one quarter of the cycle of the control signal driving the half-bridge inverter.[3]
- The difference of the amplitude of the Primary Cell voltage in the HI and LO state is at least 200 mV.

During a transition, the Primary Cell current and Primary Cell voltage are undefined. See Figure 2 and Table 4.

[1] The HI and LO states do not correspond to fixed Primary Cell current and/or Primary Cell voltage levels.

[2] The design requirements of the Mobile Device determine both the range of lateral displacements that constitute proper alignment and the range of loading conditions on its Power Receiver.

[3] The start of the cycle corresponds the closing of the top switch in the half-bridge inverter. See the *Qi Specification, Power Transmitter Reference Designs* or the applicable Power Transmitter Reference Design document.

Figure 2. Amplitude modulation of the Power Signal

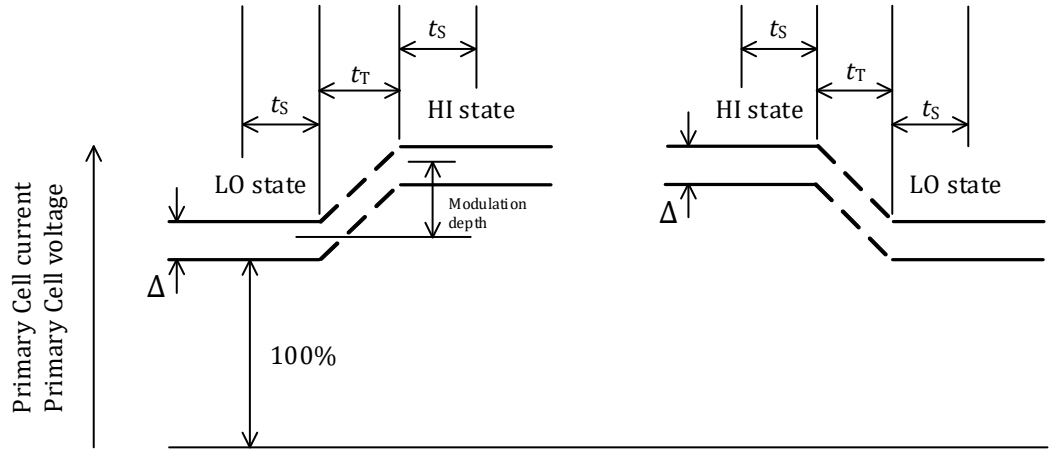


Table 4: Amplitude modulation of the Power Signal

Parameter	Symbol	Value	Unit
Maximum transition time	t_T	100	µs
Minimum stable time	t_S	150	µs
Current amplitude variation	Δ	8	mA
Voltage amplitude variation	Δ	110	mV

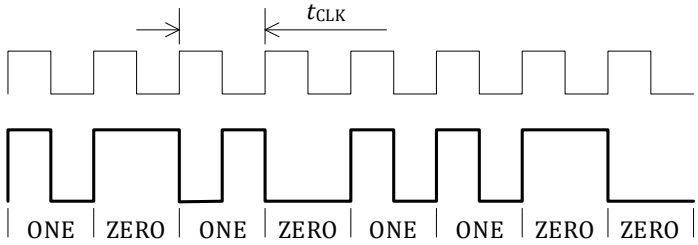
2.2 Bit encoding scheme

The Power Receiver shall use a differential bi-phase encoding scheme to modulate data bits onto the Power Signal. For this purpose, the Power Receiver shall align each data bit to a full period t_{CLK} of an internal clock signal, such that the start of a data bit coincides with the rising edge of the clock signal. This internal clock signal shall have a frequency f_{CLK} = (2 ± 4%) kHz.

NOTE: A ripple on the Power Receiver's load yields a ripple on the Power Transmitter's current. As a result, such a ripple can lead to bit errors in the Power Transmitter. The number of bit errors can be particularly high if this ripple has a frequency that is close to the modulation frequency f_{CLK}.

The Receiver shall encode a ONE bit using two transitions in the Power Signal, such that the first transition coincides with the rising edge of the clock signal and the second transition coincides with the falling edge of the clock signal. The Receiver shall encode a ZERO bit using a single transition in the Power Signal, which coincides with the rising edge of the clock signal.

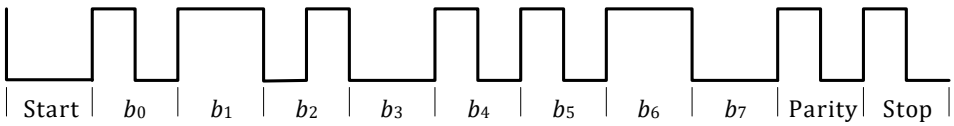
Figure 3. Example of a differential bi-phase encoding scheme



2.3 Byte encoding scheme

The Power Receiver shall use an 11-bit asynchronous serial format to transmit a data byte. This format consists of a start bit, the 8 data bits of the byte, a parity bit, and a single stop bit. The start bit is a ZERO. The order of the data bits is LSB first. The parity bit is odd. This means that the Power Receiver shall set the parity bit to ONE if the data byte contains an even number of ONE bits. Otherwise, the Power Receiver shall set the parity bit to ZERO. The stop bit is a ONE. Figure 4 shows the data byte format—including the differential bi-phase encoding of each individual bit—using the value 0x35 as an example.

Figure 4. Example of the asynchronous serial format

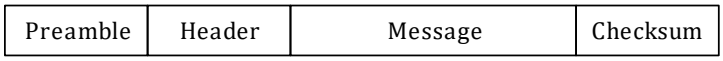


2.4 Data packet structure

The Power Receiver shall communicate to the Power Transmitter using data packets. As shown in Figure 5, a data packet consists of 4 parts, namely a preamble, a header, a message, and a checksum. The preamble consists of a minimum of 11 and a maximum of 25 bits, all set to ONE, and encoded as defined in Section 2.1, *Modulation scheme*. The preamble enables the Power Transmitter to synchronize with the incoming data and accurately detect the start bit of the header.

The header, message, and checksum consist of a sequence of three or more bytes encoded as defined in Section 2.3, *Byte encoding scheme*.[4]

Figure 5. data packet format



The Power Transmitter shall consider a data packet as received correctly if:

- The Power Transmitter has detected at least 4 preamble bits that are followed by a start bit.
- The Power Transmitter has not detected a parity error in any of the bytes that comprise the data packet. This includes the header byte, the message bytes, and the checksum byte.
- The Power Transmitter has detected the stop bit of the checksum byte.
- The Power Transmitter has determined that the checksum byte is consistent (see Section 2.4.3, *Checksum*).

If the Power Transmitter does not receive a data packet correctly, the Power Transmitter shall discard the data packet and not use any of the information contained therein.

NOTE: In the ping phase as well as in the identification and configuration phase, this typically leads to a time-out, which causes the Power Transmitter to remove the Power Signal.

2.4.1 Header

The header consists of a single byte that indicates the data packet type. In addition, the header implicitly provides the size of the message contained in the data packet. The number of bytes in a message is calculated from the value contained in the header of the data packet, as shown in the center column of Table 5.

[4] The Power Receiver should turn off its communications modulator after transmitting a data packet. This may cause an additional HI state to LO state or LO state to HI state transition in the Primary Cell current.

Table 5: Message size

Header	Message Size*	Comment
0x00…0x1F	1 + (Header – 0) / 32	1 ×32 messages (size 1)
0x20…0x7F	2 + (Header – 32) / 16	6 × 16 messages (size 2…7)
0x80…0xDF	8 + (Header – 128) / 8	12 × 8 messages (size 8…19)
0xE0…0xFF	20 + (Header – 224) / 4	8 × 4 messages (size 20…27)
* Values in this column are truncated to an integer.		

2.4.2 Message

The Power Receiver shall ensure that the message contained in the data packet is consistent with the data packet type indicated in the header. See *Qi Specification, Communications Protocol* for a detailed definition of the possible messages. The first byte of the message, byte B_0, directly follows the header.

2.4.3 Checksum

The checksum consists of a single byte that enables the Power Transmitter to check for transmission errors. The Power Transmitter shall calculate the checksum as follows:

$$C := H \oplus B_0 \oplus B_1 \oplus \ldots \oplus B_{\text{last}}$$

where C represents the calculated checksum, H represents the header byte, and B_0, B_1,..., B_{last} represent the message bytes.

If the calculated checksum C and the checksum byte contained in the data packet are not equal, the Power Transmitter shall determine that the checksum is inconsistent.

2.4.4 Correct reception of a data packet

A Power Transmitter shall decide that it has received a data packet correctly if and only if:

- the start bit and stop bits of each data byte are correct;
- the parity bit of each data byte is correct; and
- the checksum value at the end of the data packet is correct.

If the Power Transmitter has not received a data packet correctly, it shall discard the data packet and proceed as if it had not received the latter.

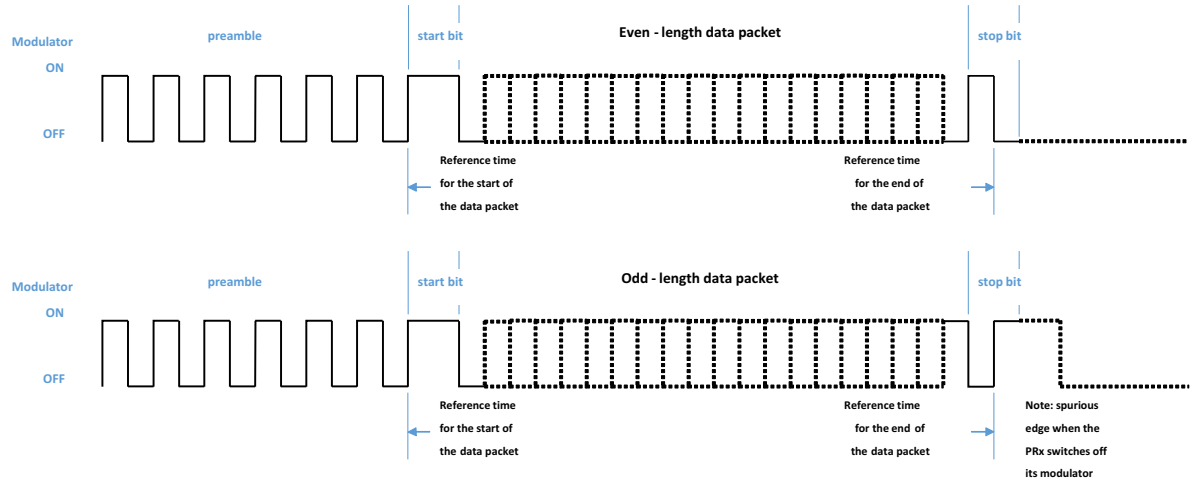
NOTE: The above requirement implies that a Power Transmitter does not respond to simple-query data packets or to data-request data packets that are incorrectly received.

2.4.5 Start and end of a data packet

Figure 6 zooms in on the start and end of a data packet, showing a number of preamble data bits, the first start bit, and the final stop bit. The reference time for the start of a data packet is the edge at the start of the first start bit (a ZERO). The reference time for the end of a data packet is the edge at the center of the final stop bit (a ONE).

After transmitting a data packet containing an odd number of data bytes, the communications signal contains an additional edge. This additional edge is not a part of the data packet; it results from the Power Receiver switching off its modulator.

Figure 6. Start and end of a load-modulated data packet



3 Frequency-shift keying

The Power Transmitter communicates to the Power Receiver using Frequency Shift Keying, in which the Power Transmitter modulates the Operating Frequency of the Power Signal.

This section defines both the physical layer and the data link layer of the Power Transmitter to Power Receiver communications interface. The data link layer supports both data packets and Responses. The format of a data packet is defined in Section 3.3, *Byte encoding scheme*. The format of a Response is defined in Section 3.5, *Response Pattern*.

3.1 Modulation scheme

The Power Transmitter shall switch its Operating Frequency between the Operating Frequency f_{op} in the unmodulated state and the Operating Frequency f_{mod} in the modulated state. The difference between these two frequencies is characterized by two parameters:

- *Polarity.* This parameter determines whether the difference between f_{mod} and f_{op} is positive or negative.

  NOTE: In both the Configuration data packet and a Specific Request data packet that has its Request field set to 0x03 (FSK Parameters), the Power Receiver encodes the positive polarity as a ZERO and the negative polarity as a ONE. In addition, note that a negative polarity typically increases the voltage induced in the Secondary Coil, and therefore should be used with care.

- *Depth.* This parameter determines the magnitude of the difference between f_{op} and f_{mod}.

  NOTE: Both the Configuration data packet and the Specific Request data packet (Request 0x03, FSK Parameters) encode the modulation depth in a two-bit unsigned integer value.

For any given Operating Frequency f_{op}, and depending on the polarity and depth parameters, f_{mod} shall be chosen such that the time difference between a single cycle of f_{mod} and a single cycle of f_{op} is in the range that is defined in Table 6.

NOTE: The minimum time difference in this Table corresponds to a single cycle of a 32 MHz clock.

Table 6: FSK States

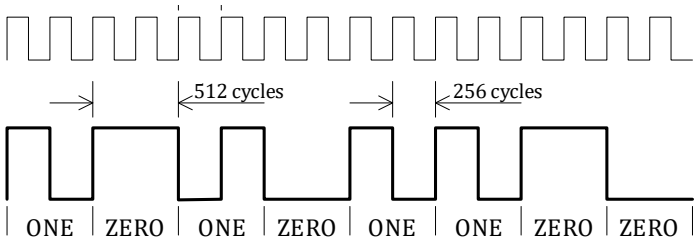
Polarity	Depth	$\frac{1}{f_{mod}} - \frac{1}{f_{op}}$		Unit
		Minimum	Maximum	
positive	3	-282.00	-249.00	ns
positive	2	-157.00	-124.00	ns
positive	1	-94.50	-61.50	ns
positive	0	-63.25	-30.25	ns
negative	0	30.25	63.25	ns
negative	1	61.50	94.50	ns
negative	2	124.00	157.00	ns
negative	3	249.00	282.00	ns

3.2 Bit encoding scheme

The Power Transmitter shall use a differential bi-phase encoding scheme to modulate data bits in the Power Signal. For this purpose, the Power Transmitter shall align each data bit to 512 cycles of the Power Signal frequency.

The Power Transmitter shall encode a ONE bit using two transitions in the Power Signal frequency. The first transition shall occur at the start of the bit and the second transition shall occur at 256 cycles into the bit. The Transmitter shall encode a ZERO bit using a single transition in the Power Signal frequency at the start of the bit.

Figure 7. Example of differential bi-phase encoding



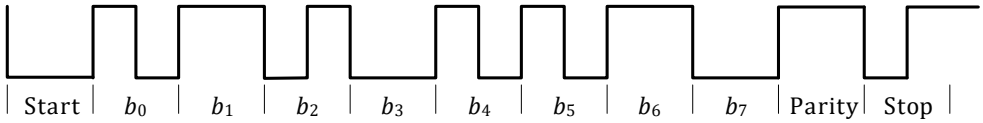
3.3 Byte encoding scheme

The Power Transmitter shall use an 11-bit asynchronous serial format to transmit a data byte. This format consists of a start bit, the 8 data bits of the byte, a parity bit, and a single stop bit. The start bit is a ZERO. The order of the data bits is LSB first. The parity is even, which means that the Power Transmitter shall set the parity bit to ONE if the data byte contains an odd number of ONE bits. Otherwise, the Power Transmitter shall set the parity bit to ZERO.

NOTE: For clarity, Power Receiver to Power Transmitter communications use odd parity, as defined in the *Qi Specification, Power Delivery*.

The stop bit is a ONE. Figure 8 shows the data byte format—including the differential bi-phase encoding of each individual bit—using the value 0x35 as an example. The Power Transmitter shall send all bits in a contiguous sequence without a pause in between two consecutive bits. It shall send the start bit first and the stop bit last.

Figure 8. Example of the asynchronous serial format



3.4 Data packet structure

The Power Transmitter shall communicate to the Power Receiver using data packets. A data packet consists of a series of bytes that the Power Transmitter shall send as a contiguous sequence, i.e. there shall be no pauses in between two consecutive bytes. Section 3.4.1, *Header* defines the format of a byte. As shown in Figure 9, a data packet consists of three parts, a header, a message, and a checksum. The header, message, and checksum consist of a sequence of three or more bytes encoded as defined in Section 3.4.1, *Header*.

Figure 9. Data packet format

The Power Receiver shall consider a data packet as received correctly if:

- The Power Receiver has not detected a parity error in any of the bytes that comprise the data packet. This includes the header byte, the message bytes and the checksum byte.
- The Power Receiver has detected the stop bit of the checksum byte.
- The Power Receiver has determined that the checksum byte is consistent (see Section 3.4.3, *Checksum*).

If the Power Receiver does not receive a data packet correctly, the Power Receiver shall discard the data packet and not use any of the information contained therein.

3.4.1 Header

The header consists of a single byte that indicates the data packet type. In addition, the header implicitly provides the size of the message contained in the data packet. The number of bytes in a message is calculated from the value contained in the header of the data packet, as is shown in the center column of Table 7.

Table 7: Message size

Header	Message Size*	Comment
0x00 to 0x1F	1 + (Header – 0) / 32	1 ×32 messages (size 1)
0x20 to 0x7F	2 + (Header – 32) / 16	6 × 16 messages (size 2 to 7)
0x80 to 0xDF	8 + (Header – 128) / 8	12 × 8 messages (size 8 to 19)
0xE0 to 0xFF	20 + (Header – 224) / 4	8 × 4 messages (size 20 to 27)
* Values in the Message Size column are truncated to an integer.		

3.4.2 Message

The Power Transmitter shall ensure that the message contained in the data packet is consistent with the data packet type indicated in the header. See *Qi Specification, Communications Protocol* for a detailed definition of the possible messages. The first byte of the message, byte B_0, directly follows the header.

3.4.3 Checksum

The checksum consists of a single byte that enables the Power Receiver to check for transmission errors. The Power Transmitter shall calculate the checksum as follows,

$$C := H \oplus B_0 \oplus B_1 \oplus \ldots \oplus B_{\text{last}}$$

where C represents the calculated checksum, H represents the header byte, and B_0, B_1,..., B_{last} represent the message bytes.

If the calculated checksum C and the checksum byte contained in the data packet are not equal, the Power Receiver shall determine that the checksum is inconsistent.

3.4.4 Correct reception of a data packet

A Power Receiver shall decide that it has received a data packet correctly if and only if:

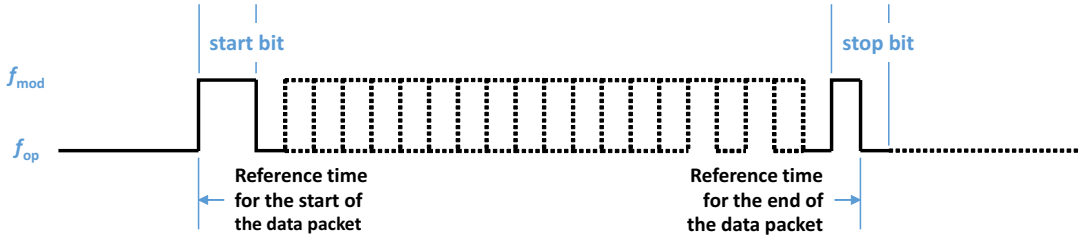
- the start bit and stop bits of each data byte are correct;
- the parity bit of each data byte is correct; and
- the checksum value at the end of the data packet is correct.

If the Power Receiver has not received the data packet correctly, it shall discard the data packet and proceed as if it had not received the latter.

3.4.5 Start and end of a data packet

Figure 10 zooms in on the start and end of a data packet, showing the first start bit and the final stop bit. The reference time for the start of a data packet is the edge at the start of the first start bit (a ZERO). The reference time for the end of a data packet is the edge at the center of the final stop bit (a ONE).

Figure 10. Start and end of an FSK data packet



3.5 Response Pattern

When a Power Receiver sends a simple query data packet (see *Qi Specification, Communications Protocol* for the classification of data packets a Power Receiver can send), the Power Transmitter responds with a Response Pattern. Table 8 and Figure 11 define the four possible eight-bit Response Patterns.

NOTE: Unlike a data byte, a Response Pattern does not include a start bit, a parity bit, and a stop bit. Due to its structure, a Power Receiver can use relatively simple decoding logic to distinguish between the Response Patterns.

Table 8: Response Patterns

Response Pattern	Description
ACK	Acknowledge
NAK	Not acknowledge
ND	Not defined
ATN	Attention

Figure 11. Format of the Response Patterns